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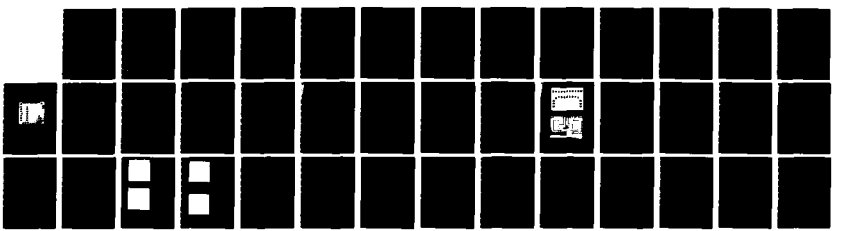

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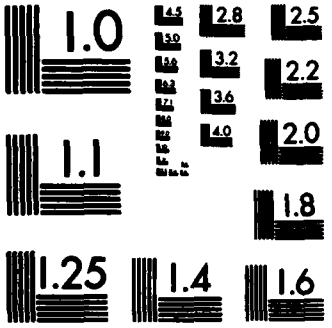

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Interim Report

INTEGRATION OF DETECTORS WITH OPTICAL WAVEGUIDE STRUCTURES

J. T. Boyd

Solid State Electronics Laboratory
Department of Electrical and Computer Engineering
University of Cincinnati
Cincinnati, Ohio 45221

J. T. Boyd, Principal Investigator

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Progress in several areas regarding the integration of photodetector arrays with optical waveguide structures is presented. A photosensor element suitable for incorporation into charge-coupled device (CCD) imaging arrays in which the charge injected into the CCD is proportional to the logarithm of incident light intensity has been successfully demonstrated. The photosensor element consists of a photodiode directly coupled to a two stage MOSFET common source amplifier. This element occupies an area of 25 μm x 100 μm and is arranged so that it could be incorporated into a linear CCD imaging

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array having a period of 25 μm. A logarithmic response is measured over a 68.6 dB range of incident light intensity with a sensitivity of 55 mV per decade of light intensity. The concept of illuminating a silicon photodetector along an edge to increase the light propagation path through the depletion region and thus to increase quantum efficiency at near infrared wavelengths has also been successfully demonstrated. Quantum efficiency measurements using both a GaAlAs laser and a HeNe laser are included. These measurements show an improvement in quantum efficiency at $\lambda = 0.83$ μm for edge illumination over normal incidence of 75% for a photodiode and of 142% for a MOS capacitor photosensor. A three gate MOS transistor has also been demonstrated. Measurements of operating characteristics illustrate the availability of excellent control of the transconductance while simultaneously maintaining very high output resistance. In analog circuit applications the three gate device provides additional advantages including better signal isolation, less nonlinearity, and adjustable mismatch in a differential amplifier. A range of operating voltages over which the transconductance is constant is observed. Progress achieved in implementing very low scattering graded-index SiO_2 waveguides and the integration of laser-recrystallized photodetector arrays on $LiNbO_3$ is also included.

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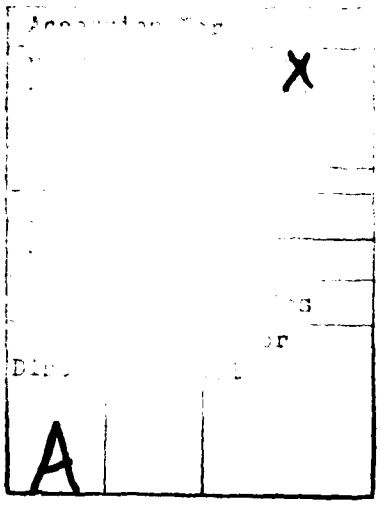

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I. Introduction

We are currently performing research under grant AFOSR 81-0130 involving integration of a detector array with an optical waveguide structure and applications to signal processing. This grant is continuing research initiated under grant AFOSR 76-3032; results from this earlier grant are described in the final report.[1] The present report summarizes progress achieved in Part II of this research program (March 15, 1982 - March 14, 1983). The main accomplishments resulting from research performed during this period include a number of accomplishments in the area of photodetectors and their integration into optical waveguide structures[2-4] and continued progress on graded index SiO_2 waveguides having very low scattering loss.[5-6] In the area of photodetectors success has been achieved in the implememtation of a log converting array sensor element for charge-coupled device (CCD) image arrays and demonstration of the advantages of edge detection of long wavelength radiation by silicon photodetectors. Results in each of these areas are discussed in the following sections.

The present research program has thus far investigated a number of integrated optical device configurations utilizing a silicon substrate. The motivation for investigating devices utilizing silicon is first, due to its potential use for such signal processing devices as the integrated optical spectrum analyzer,[7-10] second, its usefulness for performing waveguide detection in such signal processing devices formed on $LiNbO_3$, third, to provide integration of external components in fiber optic interferometric devices,[11] and fourth, to allow combination of integrated optical devices and integrated electronic circuits to form

higher data rate systems. The recent demonstration in our laboratory of waveguide loss in thin film waveguides as low as .01 dB/cm after laser annealing implies that it may be worthwhile considering formation of the interferometer in an optical waveguide rather than a fiber.[11] Such a configuration would significantly reduce the size and allow total component integration on a silicon wafer substrate. This reduction in size and increase in component integration would be very desirable for application of guided wave interferometric sensors in military systems.

To support the overall goals of Air Force research, there has been significant interaction between personnel involved in the present and past AFOSR research program and those involved in military programs at the Air Force Avionics Laboratory, Rockwell International, McDonnell-Douglas, Battelle, Motorola, General Dynamics, Lockheed, Honeywell, and Oak Ridge National Laboratory. A number of papers have been co-authored by personnel from several of these institutions with personnel from the Solid State Electronics Laboratory at the University of Cincinnati.

II. Photodetectors

A. Log-Converting Photosensor Element for CCD Linear Imaging Arrays

Charge-coupled device (CCD) imaging arrays generally consists of either silicon gate MOS capacitor photosensors or photodiodes coupled in parallel to a CCD.[12] The output of these imaging arrays is linearly proportional to incident light intensity over a limited range of light intensity. In some applications it would be advantageous to have a monotonic response over a much larger range of light intensity, even if linearity were to be sacrificed. The log-converting photosensor element presented here performs such a function. This sensor element allows the charge injected into the CCD to be proportional to the logarithm of incident light intensity. The output of the CCD charge sensing amplifier is thus also proportional to the logarithm of the incident light intensity. Because of this logarithmic conversion, signal charge will not fill the potential wells nor saturate the ouptut amplifier nearly as quickly as it normally would as light intensity is increased. For the log-converting photosensor being presented here we demonstrate a logarithmic response over nearly seven decades of incident light intensity, a much larger range of response than that for CCD imagers with conventional photosensor elements.[13]

The log-converting photosensor element including the structure coupling it to a CCD being presented here includes the addition of several transistors as opposed to conventional sensors and coupling structures. These transistors implement the log conversion. Their presence causes an elongation of the area occupied by the sensor and coupling structure in the direction perpendicular to the axis of a

linear CCD imaging array, but not in the direction parallel. Resolution of a linear imaging array would thus not be affected.

A block diagram and the circuit design for the log-converting CCD sensor element are shown in Figure 1 and Figure 2, respectively. In this structure, there are three stages: (1) The input amplifier which is especially designed for a photodiode without any coupling capacitor to achieve the gain and level shifting requirement. (2) The CCD stage where the potential equilibration method is employed. (3) The output source follower where an on-chip depletion mode load MOSFET is used. The photodiode can be operated in either reverse biased or open circuit condition. The volt-ampere characteristic of the photodiode is given by [14]

$$I = I_s + I_o(1 - e^{\frac{qV}{mkT}}) \tag{1}$$

where I_s, the short-circuit current, is proportional to the light intensity, I_o is the reverse saturation current of a diode, and I and V are the current through and voltage across the photodiode. If a reverse biased p-n junction is illuminated, the current varies almost linearly with the light flux. If the photodiode is open circuited, the current I flowing in the circuit is zero. With this condition and Eq. (1), the photovoltaic voltage across the photodiode becomes

$$V = \frac{mkT}{q} \ln \left(\frac{I_o+I_s}{I_o}\right) \tag{2}$$

Since, except for very small light intensities, $I_s/I_o >> 1$, V increases logarithmically with I_s, and hence with illumination as given by

$$V = \frac{mkT}{q} \ln \left(\frac{I_s}{I_o}\right) \tag{3}$$

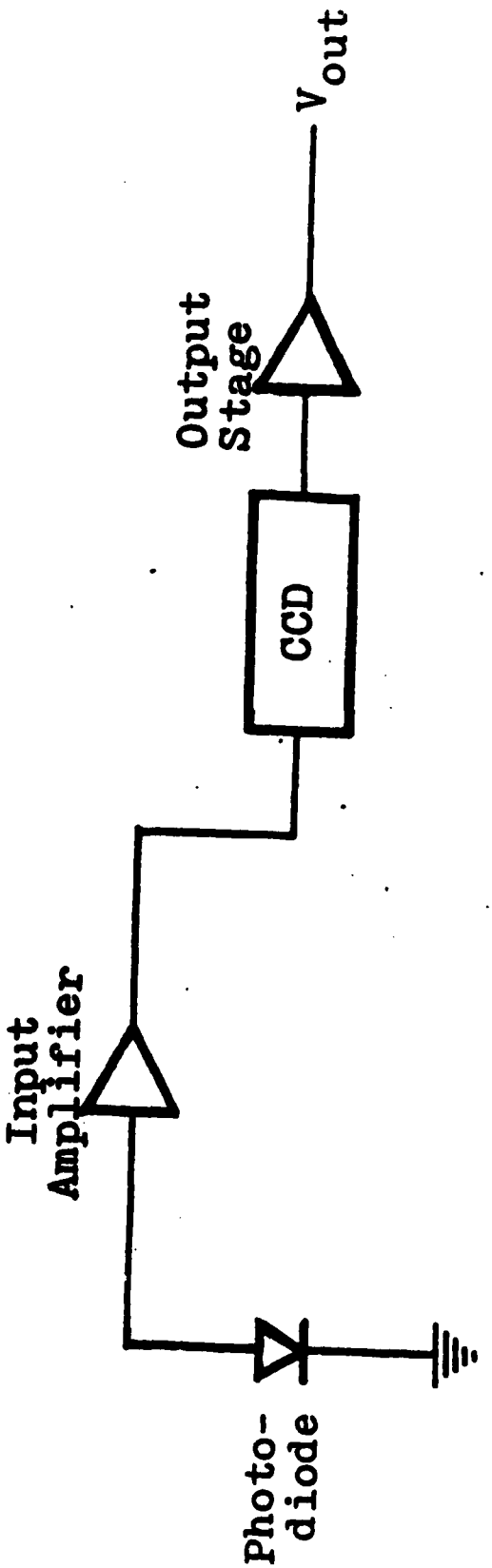


Figure 1. Block diagram of the log-converting CCD sensor element.

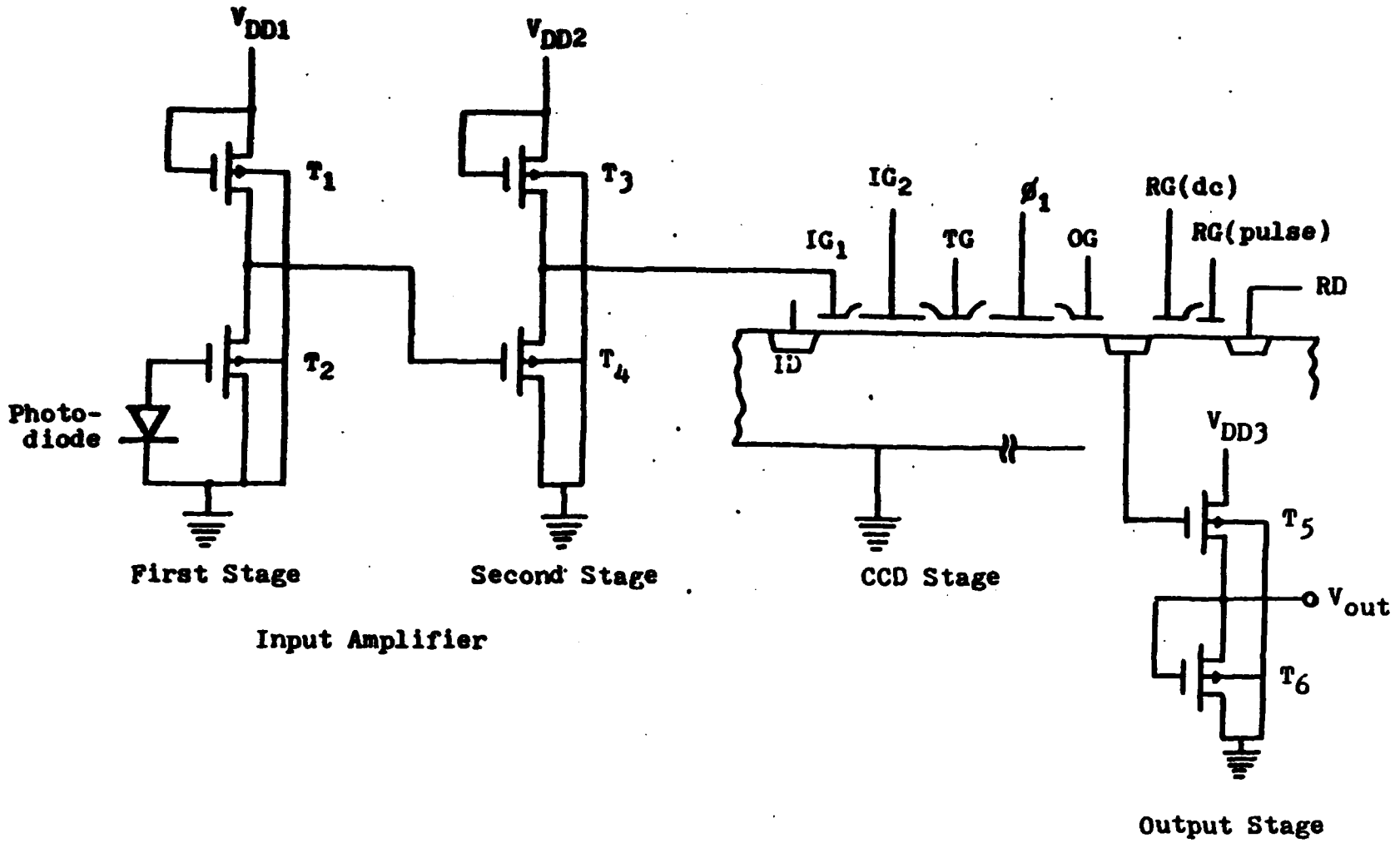


Figure 2. Circuit diagram of the log-converting CCD sensor element.

The input amplifier has two cascade common source (CS) amplifiers with an enhancement mode load MOSFET. The photodiode is connected directly to the input of the driver of the first stage inverter. In order to eliminate the coupling capacitor and bias circuitry, the driver of the first stage inverter has to be a depletion mode MOSFET. The second stage CS amplifier is an enhancement mode load and driver pair. By cascading these two CS amplifiers together, the overall transfer function of the input amplifier is

$$V_{out} = V_{DD2}-V_{T3} - A_{V2} \cdot (V_{DD1} - V_{T1} - V_{T4})+ A_{V1} \cdot A_{V2} (V_{in}-V_p) \quad (4)$$

where $A_{V1} = \sqrt{(W/L)_{D1}/(W/L)_{L1}}$ and $A_{V2} = \sqrt{(W/L)_{D2}/(W/L)_{L2}}$ are the gains of the first and second stages of the amplifier shown in Figure 2, V_p is the threshold voltage of the depletion mode MOSFET T_2, V_{Ti} is the threshold voltage for the ith transistor, $(W/L)_{Di(Li)}$ is the width-to-length ratio of the driver (load) transistor of the ith stage, and other parameters are defined in Figure 2. It is obvious that the input amplifier not only gives the desired operational point which the succeeding CCD stage needs but also amplifies the photodiode output signal by $A_{V1} \cdot A_{V2}$. The output signal of the input amplifier is directly connected to the first input gate (IG1) so that the charge injected into the potential well beneath the second input gate (IG2) from the injecting diode (ID) would be proportional to the IG1 gate voltage. The size of the photosensor element plus the coupling structure is 25 μm x 100 μm configured so that it would be incorporated into a linear array having a period of 25 μm. The remaining parts of the test device are a CCD with only one electrode (i.e., ϕ_1) and output circuitry. We feel

that one photosensor element and a portion of one CCD stage coupled to a CCD output amplifier is sufficient to demonstrate log conversion, although it prevents an evaluation of array characteristics such as uniformity. Feeding the charge collected under the single CCD electrode to a sensing amplifier, which is a source follower, and measuring the output voltage allows experimental verification of the logarithmic relation.

The device is fabricated on a n-type, <100> wafer with resistivity 8 Ω-cm. The depletion mode MOSFET can be obtained by an ion implantation process where the impurities can penetrate the gate oxide and stop in the silicon surface region. An alternative approach is a non-ion implantation process. The polysilicon gate of the depletion mode MOSFET is boron doped and it is covered by a thermally grown silicon dioxide layer on the top of the polysilicon electrode. The wafer then undergoes hydrogen annealing with 24 l/min. hydrogen at 1000°C for 30 minutes. The boron impurities which are already in polysilicon then diffuse through the gate oxide to the channel. As a result a depletion mode MOSFET is formed since the boron diffusion constant in SiO_2 is much faster in H_2 ambient that that in N_2 ambient. The double layer polysilicon electrode structures for the CCD stage are both phosphorus diffused. The gate oxide is 0.15 μm. The threshold voltage of the first level and second level enhancement mode MOSFET is -1.6 volts, and that of the depletion mode MOSFET is +3 volts. A photograph of this test device is shown in Figure 3.

The log-converting CCD sensor element consists of three blocks as shown in Figure 1. The output of each block has to be in the

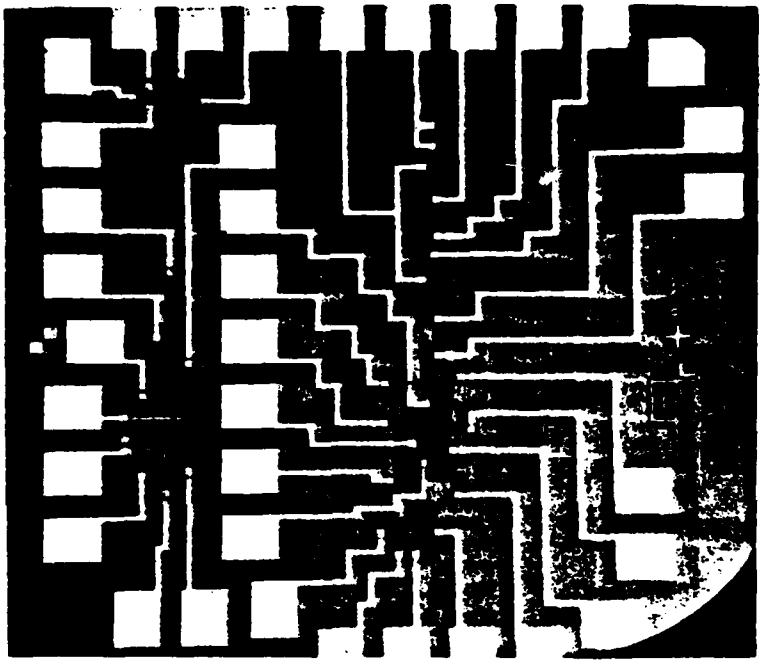


Figure 3. Photograph of log-converting CCD sensor element test circuit after fabrication.

operational range of the succeeding block. An off chip clock generator which is built up by commercially available CMOS integrated circuits is used to produce necessary clock waveforms for driving a CCD. The clock waveforms and timing diagram for the CCD stage is shown in Figure 4. The relative light intensity is measured by a photodetector (HAD-1000 made by EG&G Inc.) which consists of a photodiode and an operational amplifier. The output of this photodetector is linearly proportional to the input light intensity, and its linear range depends on the feedback resistance used in this circuit. Since the dynamic range of this commercial photodetector is small compared to the log-converting CCD sensor element, a combination of neutral density filters (NDF) and feedback resistors are used to accomplish the measurement. The beam splitter is used to vary the light intensity continuously. The NDF is calibrated by measuring several different light intensities before and after filtering and taking the average value. Once the input light intensity is measured, the commercial photodetector is removed so that the light bypasses the commercial photodetector and illuminates the log-converting CCD sensor element. With the combination of 10%, 5% and 1% NDF, we can obtain six sets of data corresponding to one measurement of the light intensity with the commercial photodetector. Each set of data is taken by adjusting the position of the log-converting CCD sensor element and the commercial photodetector so that maximum light intensity is incident on them. The resulting transfer curve of the log-converting CCD sensor element is shown in Figure 5.

For very small light intensity where I_s is comparable to or less than I_o, Eq. (2) is used instead of Eq. (3). Under this condition and

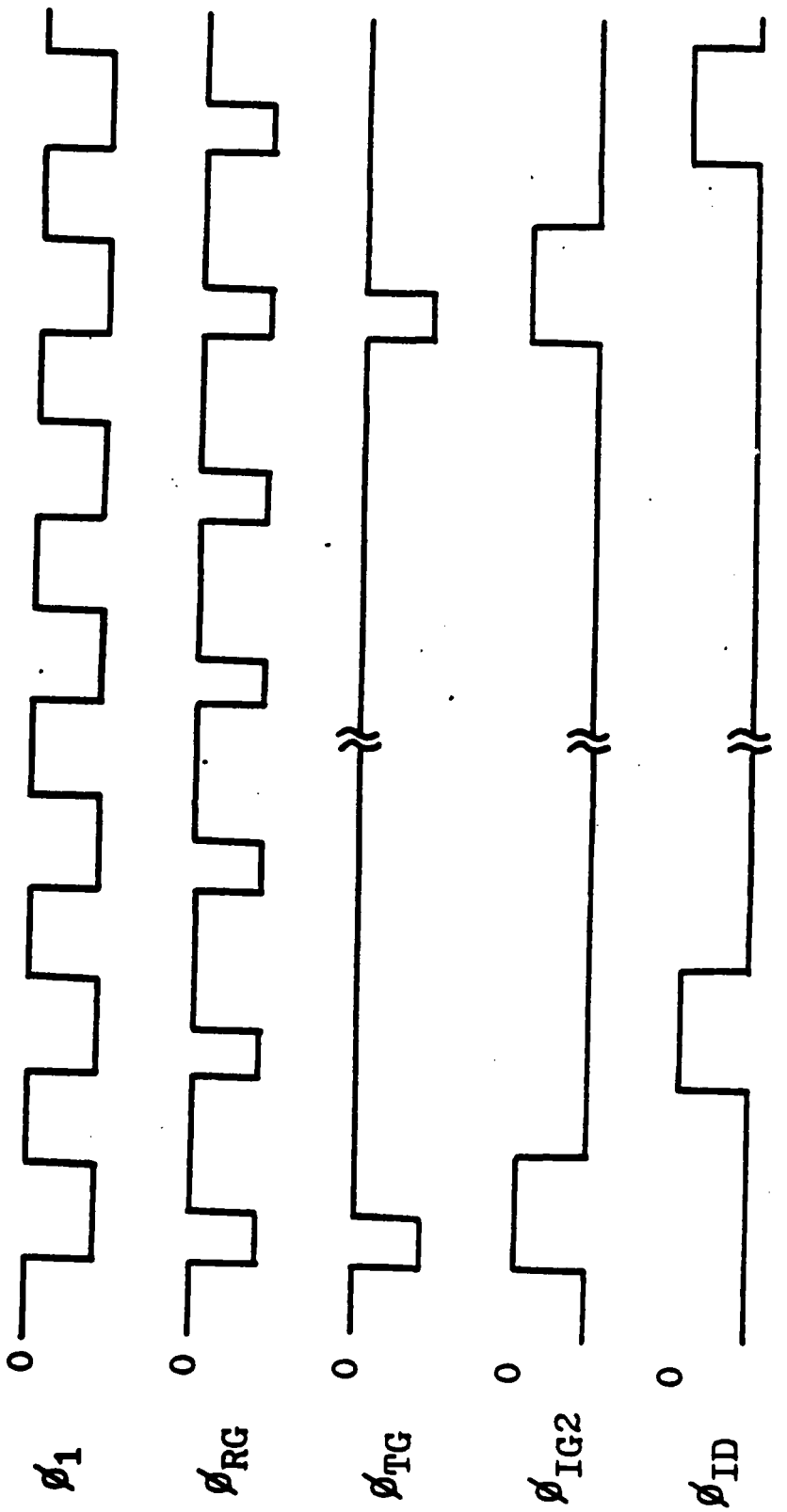


Figure 4. The clock waveforms and timing diagram for the CCD stage.

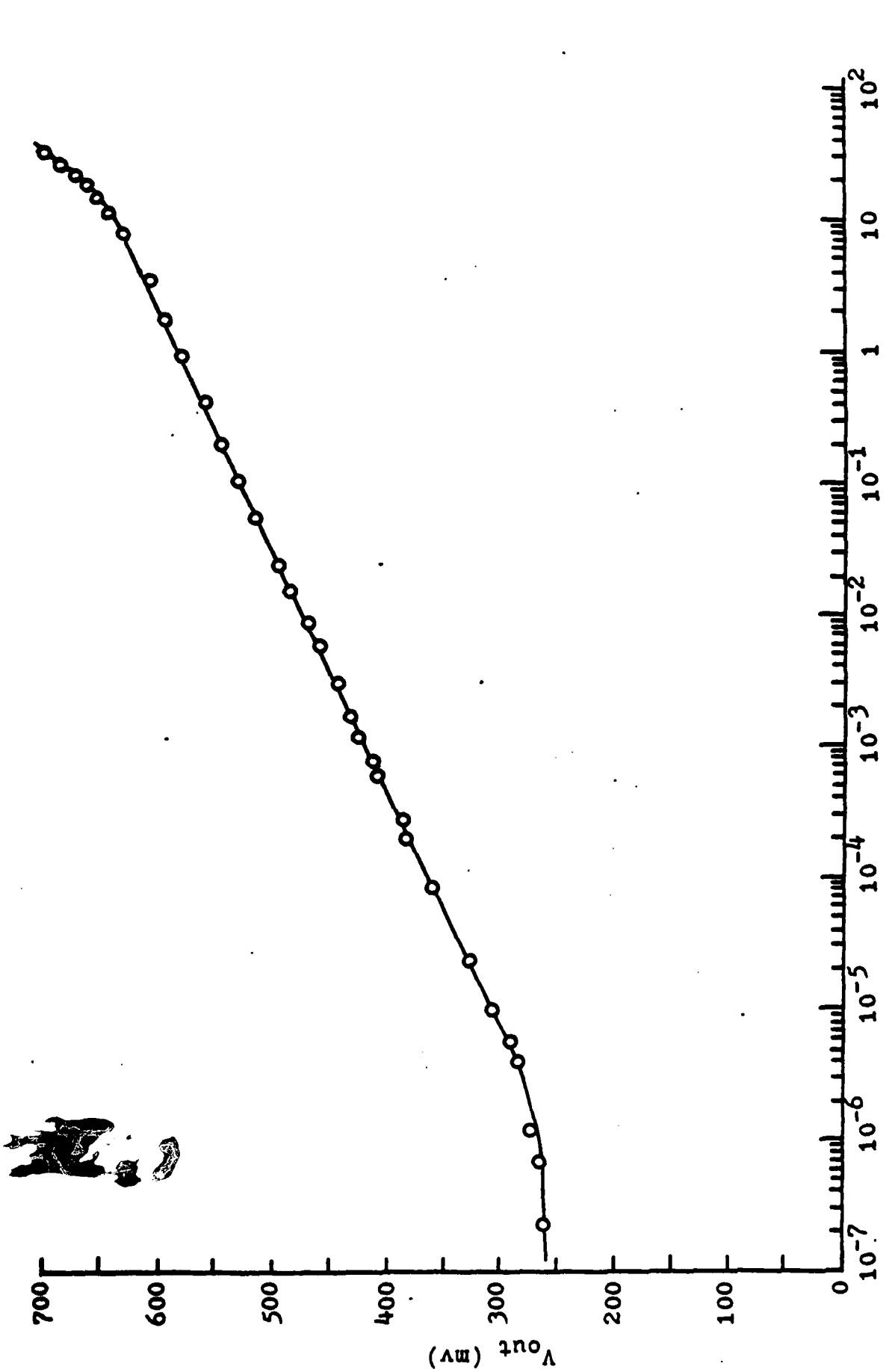


Figure 5. The transfer curve of the log-converting CCD sensor element.

subsequently decreasing the light intensity, the output asymptotically approaches 260 mV which is the output with no incident light intensity. At the mid-range of the transfer curve shown in Figure 5, the output increased logarithmically at a rate of 55 mV per decade of light intensity as input light intensity increases, until the point is reached where scattered light intensity reaching the output floating diffusion and carriers diffusing to this diffusion begin to contribute to the output waveform in a linear way. Then, as the light intensity continues to increase, the output increases rapidly and departs from the logarithmic curve. The optical power level at which scattered light begins to be a problem is about 50 microwatts. The range over which a logarithmic response is realized can be determined by the two intersections of the extrapolation of these three regions. This range is 7.29×10^6 or 68.6 dB, which is considerably larger than that of commercially available image array sensor elements.[13]

B. Improvement in the Quantum Efficiency of Silicon Photodetectors at Near IR Wavelengths by Edge Illumination

Silicon photodetectors are finding more and more applications at near infrared (IR) wavelengths as GaAlAs lasers having higher power and better beam quality become more readily available. Some of these applications involve dense arrays of silicon photosensors used for integrated optical signed processing devices.[16] High density photodetector arrays are formed by sensing elements in which the active region corresponds to a depletion region.. This depletion region may be associated with a photodiode or a MOS capacitor associated with a CCD. In dense arrays of these structures the depth of the depletion

region from the surface, and thus the active region thickness, is limited to several microns. For visible light active region sizes of several microns provide satisfactory values of quantum efficiency, but for devices operating at $\lambda = 0.83$ μm, absorption is rather weak and requires long propagation lengths through active regions to provide satisfactory values of quantum efficiency. At $\lambda = 0.83$ μm the absorption coefficient of silicon is $\alpha = 7 \times 10^2$ cm^{-1} which implies that incident light will be attenuated to 1/e of its initial value over a length of 14.3 μm.[17] To obtain a high value of quantum efficiency, a configuration having an active length exceeding this length must be utilized. We show in the present paper that by using the concept of edge illumination, large values of quantum efficiency can be obtained at $\lambda = 0.83$ μm in photosensor elements suitable for incorporation into dense arrays.

Usually light is incident on a photodetector from a direction parallel to the normal to the photodetector surface. For edge illumination light is not incident from this direction, but instead from a direction parallel to this surface. To implement edge illumination, the silicon chip on which the photodetector is found must terminate at the edge of the photodetector and this edge must be smooth. Light can then enter the photodetector from the edge. The active region length then corresponds to the photodetector sensor dimension in the direction perpendicular to the edge. Although the detector aperture is then small in one dimension, it is still sufficient for integrated optics applications.[16]

For edge illumination to be practical the position of the edge

must be precisely controlled and the resulting edge surface must be smooth. We have used a cross sectioning technique developed by us in a previous AFOSR-sponsored program which uses preferential etching of (100) oriented silicon to accurately define the axis along which fracture occurs.[18] The position of this axis is thus determined accurately by photolithography. Smooth edge surfaces corresponding to (111) planes result. Figure 6 illustrates the resulting configuration used for edge illumination.

A schematic diagram of the devices used for testing the concept of edge illumination is shown in Figure 7. Both the p-n junction photodiode and a polysilicon gate MOS capacitor are used as photodetector sensor elements. Optically generated carriers are detected by an on-chip floating diffusion amplifier. The floating diffusion is reset to a reference potential once each clock cycle by the reset drain and reset gate. The detected signal is then proportional to the variation of the floating diffusion voltage which is a function of the signal charge. Polysilicon is used as the MOS gate material because it transmits light efficiently and its use will allow a comparison of edge illumination with normal incidence illumination. A phosphorus-doped silicon wafer having a resistivity in the range of 4-9 Ω-cm with (100) surface orientation is used for test device fabrication. The wafer is thoroughly cleaned and oxidized at 1100°C in a steam atmosphere for 45 minutes to grow a 0.45 μm thick oxide layer. This layer is used as a V-groove etching mask. The V-groove is formed by preferential etching the (100) oriented silicon wafer in a 45% KOH solution at 80°C with the edge of the etching window parallel to a

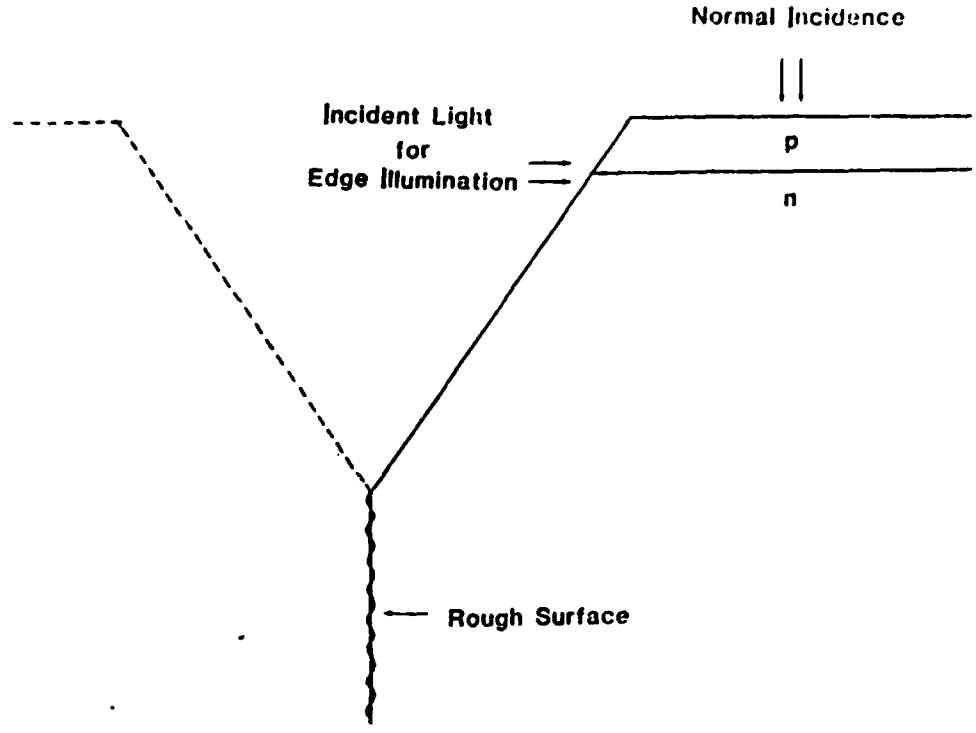


Figure 6. Photodetector configuration used for edge illumination.

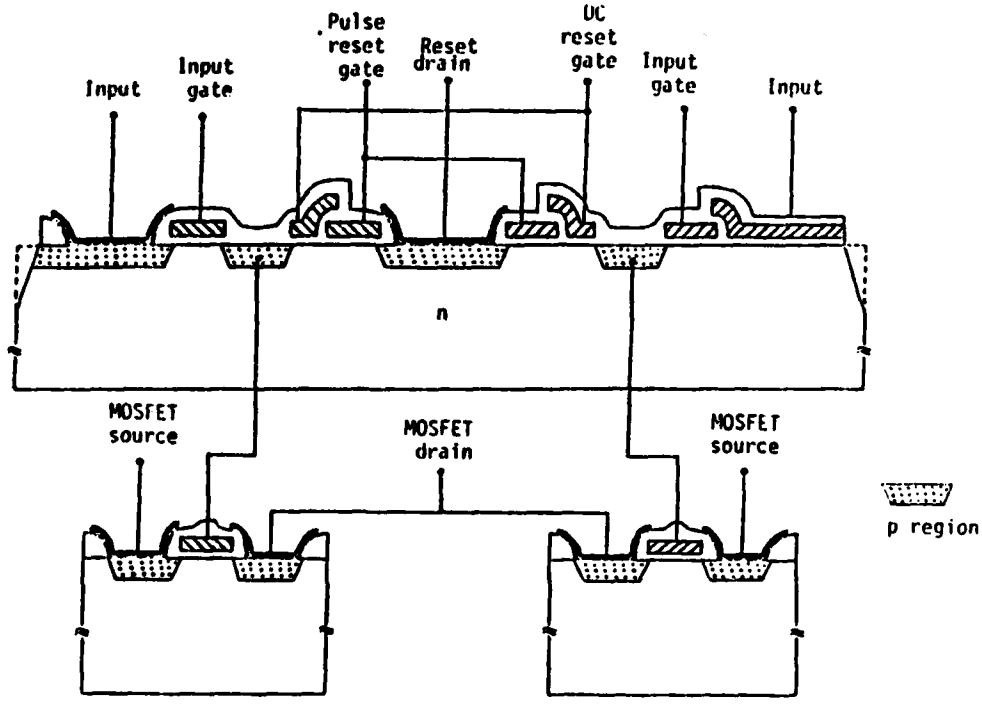


Figure 7. Photodiode and MOS capacitor sensor along with their output amplifier device configurations.

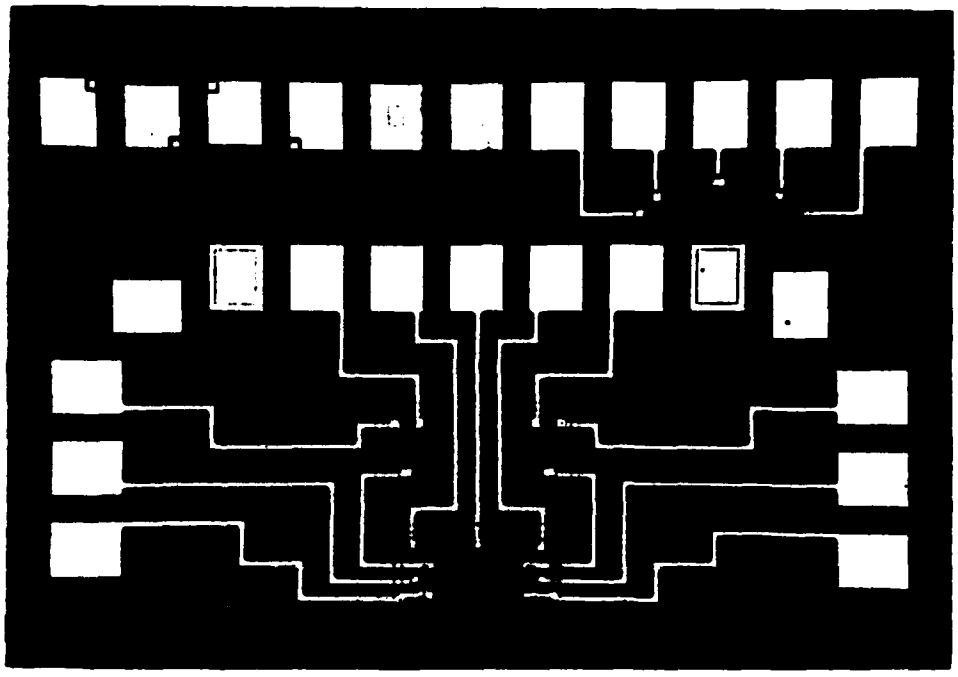
<110> direction. The resulting V-groove has sidewalls corresponding to (111) planes inclined at an angle of 54.74° with respect to the (100) surface. The width of the V-groove is designed to be 30 μm. Thus a 21.2 μm deep V-groove is obtained for the purpose of guiding breaking and eliminating requirements for cutting and polishing as indicated in Figure 6. The junction depth of the photodiode as well as the depletion width of the polysilicon gate MOS capacitor is thus much smaller than the depth of the V-groove. Conventional polysilicon gate MOS device processing is then used to fabricate the device. The polysilicon gate thickness is 0.45 μm. The completed device is shown in Figure 8. Both types of photosensors are 100 μm x 100 μm, a size larger than the usual size of photosensor array elements. The larger size does, however, ease requirements on the performance of accurate quantum efficiency measurements.

Quantum efficiency η is defined as the number of electronhole pairs collected per photon for the photodetectors, expressed as [19]

$$\eta = (I_p/q)/(P/h\nu) \tag{5}$$

where h is Plank's constant, ν is the frequency of the light source, q is electronic charge, and I_p is the photogenerated current due to the absorption of incident optical power P at wavelength λ. The term I_p is determined for the device in Figure 7 as follows. The value of the output amplifier load voltage change ΔV_o due to the presence of incident light is determined by measurement. The output transistor gain A_v is then used to determine the corresponding voltage change ΔV_G on the gate of the output transistor as

$$\Delta V_G = \Delta V_o/A_v \tag{6}$$



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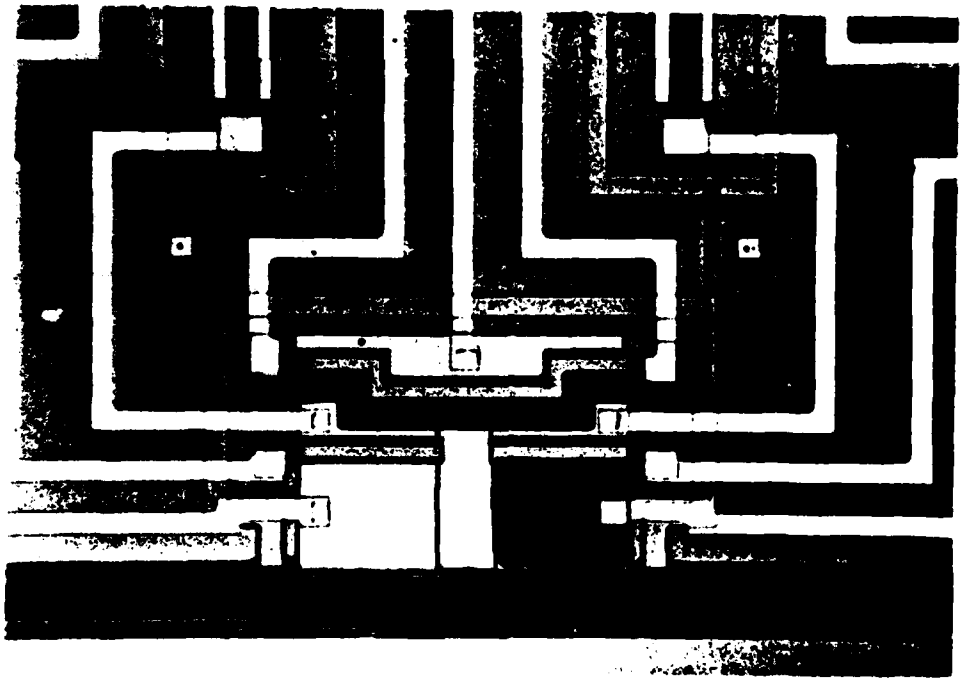


(b)

Figure 8. Photographs of the fabricated device configuration shown schematically in Figure 7. (a) 3.5X, (B) 10X.

The corresponding signal charge Q_s is proportional to ΔV_G by the relation

$$Q_s = \Delta V_G \, C_e \tag{7}$$

where C_e is the total capacitance of the floating diffusion p-n junction in parallel with the output transistor MOS gate. The effective current generated by the signal charge depends on the integration time Δt of the input gate:

$$I_{eff} = Q_s/\Delta t \tag{8}$$

Since this is the current due to the presence of light, $I_p \approx I_{eff}$. The next step is to determine the amount of incident optical power. An EG&G HAD-1000A photodiode is used as a calibrated reference to determine the total input power absorbed by the photodetectors on the test device. A collimated and focused laser beam which has passed through a beam splitter and two lenses with focal lengths of 5.6 mm and 17 mm is then allowed to be incident on this reference detector. A RCA 6032 image converter and a precision three-dimensional motion stage were used to precisely position the focused spot of the incident laser on the active region along the edge of the photodetector. Using the characteristics of responsivity for the HAD-1000A photodiode,[20] the incident power is determined. This same amount of incident power is then delivered to the photodetectors on the test device.

To provide the input optical signal, a Mitsubishi ML-3001 GaAlAs laser diode is used as the incident radiant source. It emits light as about 0.83 μm wavelength. To demonstrate the achievement of quantum efficiency improvement by means of edge illumination at $\lambda = 0.83$ μm, similar measurements have been made with a Spectra-Physics

model 145 He-Ne laser operating at $\lambda = 0.63$ μm. Since the absorption coefficient for silicon at $\lambda = 0.63$ μm is rather high ($\alpha = 3.8 \times 10^3$ cm^{-1}), it is anticipated that the quantum efficiency at this wavelength should be nearly the same using either method of light incident on the photodiode.

Table I lists the results of the quantum efficiency measurements performed on both photodiode and MOS capacitor sensors at both laser wavelengths for edge illumination and normal incidence. As expected, we see a significant improvement by using edge illumination for both types of photosensors at $\lambda = 0.83$ μm in comparison to normal incidence. In contrast little change in quantum efficiency at $\lambda = 0.63$ μm is seen for the two methods of illumination for the photodiode. The measurements reported in Table I indicate that edge illumination has an additional advantage for use with the MOS capacitor photodetector. The data indicates that for this photosensor element, edge illumination provides improvement in quantum efficiency for visible radiation. For this case the use of edge illumination avoids the loss of light in the polysilicon gate and that due to multiple reflections occuring in the multilayer MOS structure associated with normal incidence. We would expect that this quantum efficiency enhancement associated with edge illumination would be even greater in the blue region of the spectrum because of the large absorption of polysilicon in this region.

C. Three-Gate MOSFET Providing Independent Control of Transconductance and Output Resistance

In our investigation of the integration of photodetectors with

TABLE I

Quantum efficiency obtained for different cases

	Quantum Efficiency					
	Photodiode			MOS Capacitor		
	Edge Illumination	Normal Incidence	% of Increase	Edge Illumination	Normal Incidence	% of Increa
λ = 0.83 μm	0.63	0.36	75%	0.63	0.26	142%
λ = 0.63 μm	0.63	0.60	5%	0.63	0.31	103%

optical waveguide structures we have implemented various types of CCD imagers and supporting circuitry. As a part of that investigation we have encountered a limitation of MOSFETs in analog applications and overcome this limitation with the innovation of a 3-gate MOS transistor. Specifically, the finite output resistance of the MOSFET in the saturation region prevents the channel length reduction comparable with those used in digital circuits. The nonlinearity of the depletion mode load inverter pair due to the inherent square law I-V characteristics of the driver limits the dynamic range. The dual gate MOSFET [21] can reduce the Miller feedback capacitance and output conductance, but it can hardly control the transconductance g_m while at the same time maintaining a high output resistance in the saturation region. A modified version of the dual gate MOSFET has also been previously demonstrated to provide better threshold control in small devices, [22] the novel three gate device presented here can not only reduce the Miller feedback capacitance and output conductance, but also has an adjustable transconductance so that it can be operated in a certain range where the transconductance is a constant value independent of the input gate voltage. On the other hand, the input signal applied to this device is shielded by the other two DC biased gates near the source and drain ends, the resulting signal isolation is another advantage for analog IC applications.

The three gate device shown in Fig. 9 is fabricated by a six-mask process using double layer polysilicon technology. The substrate resistivity of the starting n-type, (100) wafer is 8 Ω -cm, the junction depth after fabrication is around 1.8 μm and the gate oxide

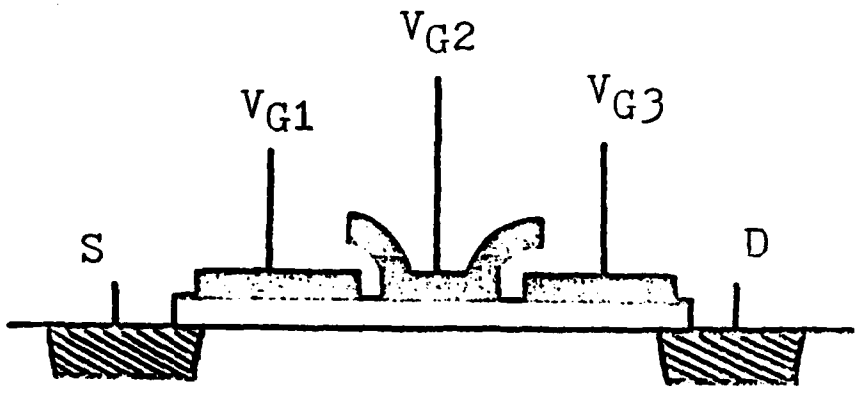


Figure 9. Schematic illustration of the cross section of the three-gate MOSFET.

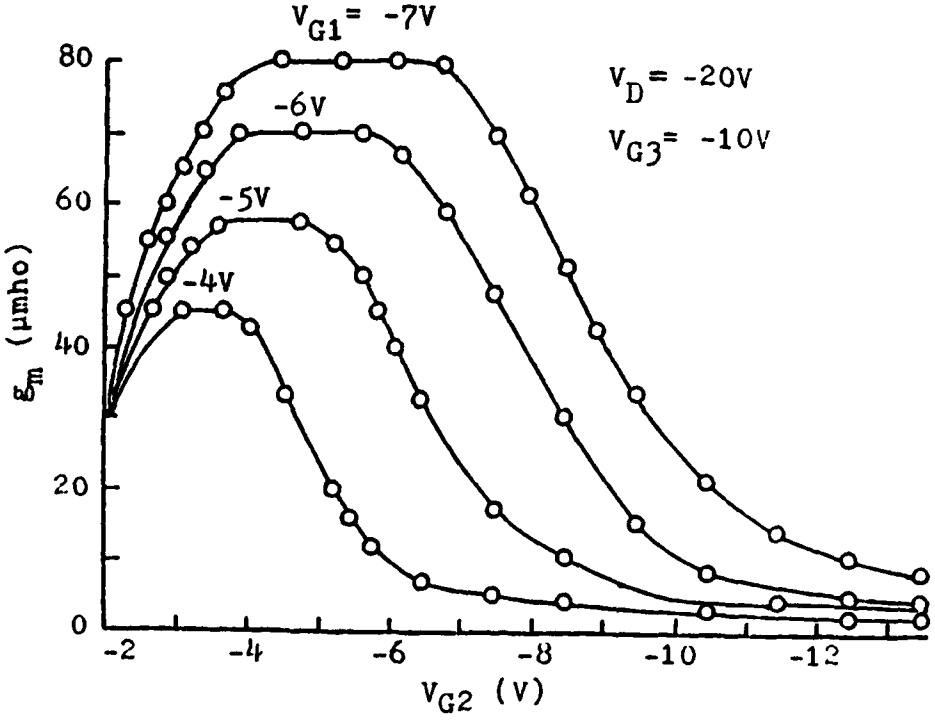
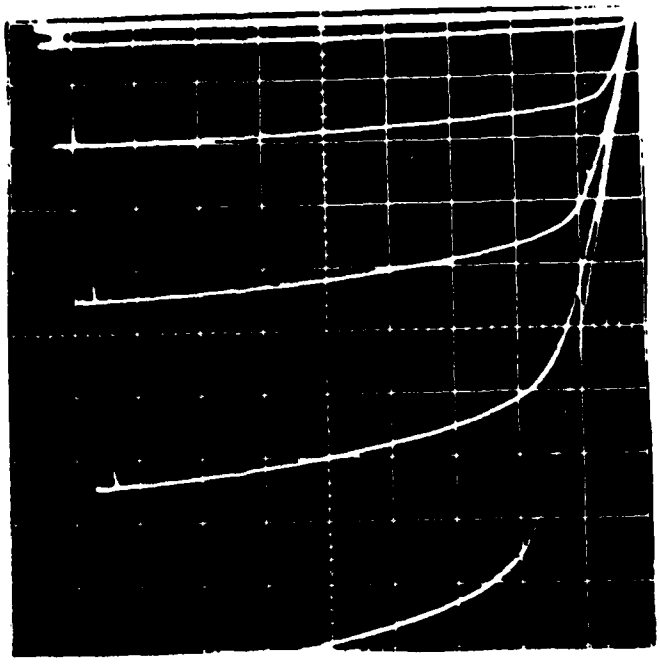
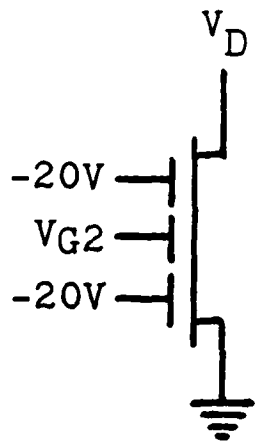


Figure 11. Transconductance g_m versus input gate voltage V_{G2} with V_{G1} a parameter.

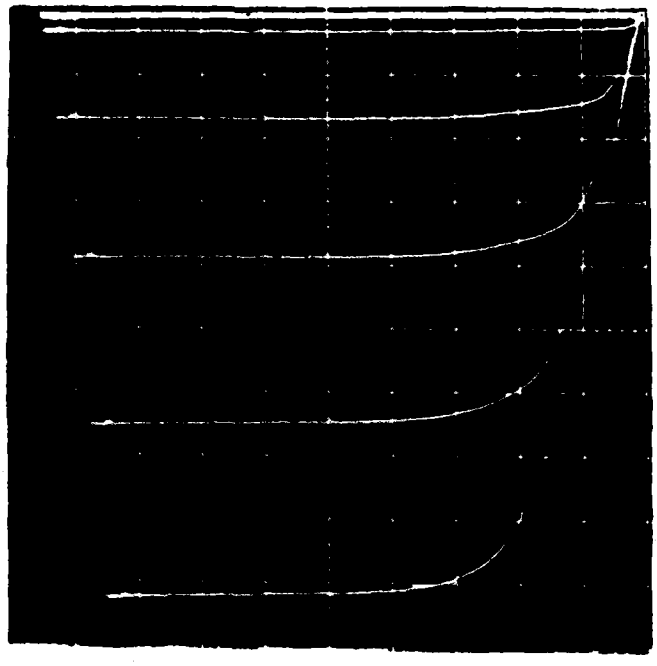
thickness is 0.15 μm. The measured channel length under G1, G2, G3, are 10.9μm, 7.6μm, and 5.8μm respectively, and the channel width is 109 μm. The three gate device can be considered as three MOSFETs connected in series with two inverted source/drains. These two inverted source/drains are located at the gap of G1 and G2 and G3 respectively. The dimension of the gap is the thickness of SiO_2 grown on polysilicon during the thermal growth of the second level gate oxide. To be a useful device, each gate of the three gate device has its own functional purpose and has to be biased properly. The gate G1 is used to adjust the transconductance, the gate G3 is used to maximize the output resistance, and the gate G2 is used as an input terminal so that the input signal is isolated.

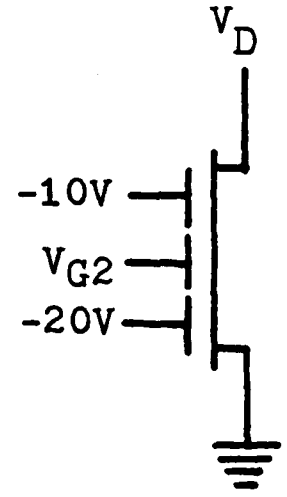
Fig. 10 shows a set of I-V characteristics of the three gate device with different bias conditions on gates G1 and G3. In Fig. 10(a), both G1 and G3 are biased at -20 volts and the voltage applied on G2 varies from -2.2 volts to -6.2 volts and 1 volt/step. As the drain voltage V_D decreases from zero to -20 volts, the channel under G2 becomes pinched off first at the inverted drain end. Since the channel under gates G1 and G3 remains in the triode region, most of the voltage drop across source and drain occurs across the channel under gate G2. Hence the finite output resistance in the saturation region is due to the channel length modulation under gate G2. This channel length modulation can be significantly reduced by increasing the bias voltage applied on gate G3 as long as the drain current I_D is not limited by the channel under gate G3, as shown in Fig. 10(b). The flatness of the output characteristics indicates that the output resistance can





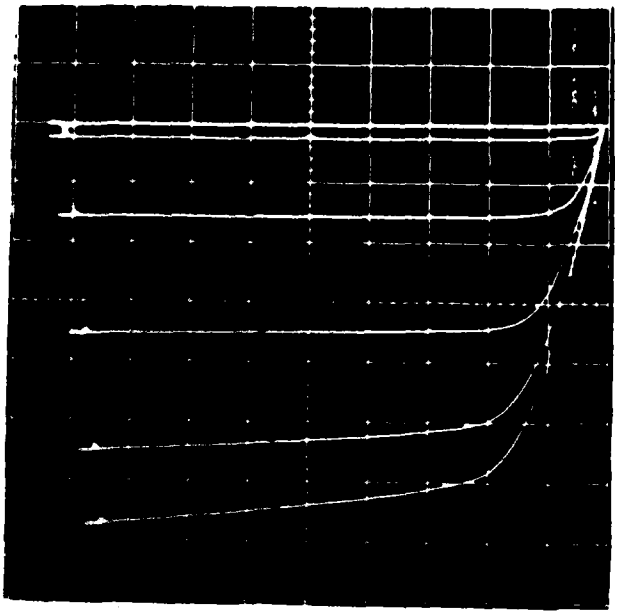
(a)

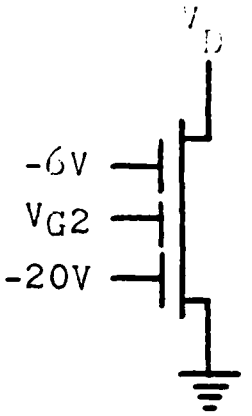




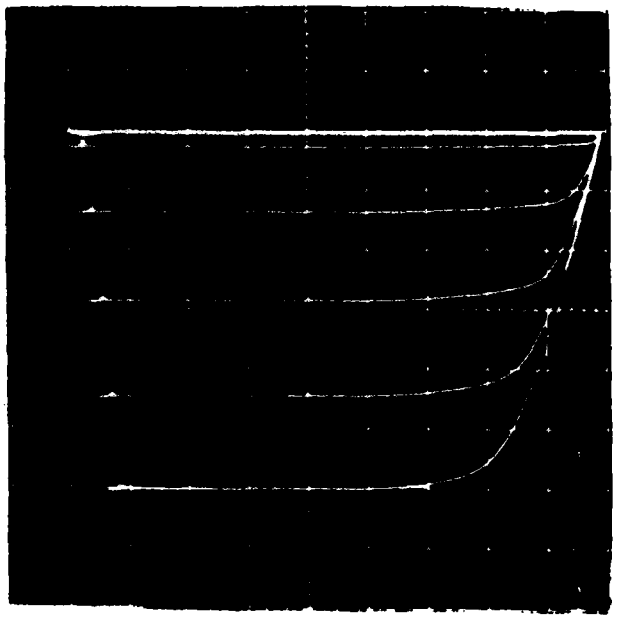
(b)

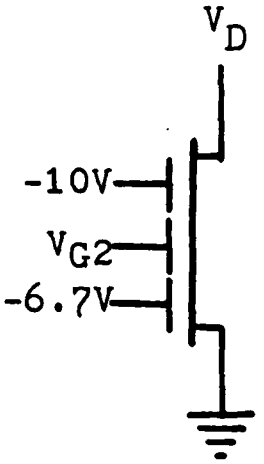
Figure 10. Output characteristics of the three gate MOSFET showing drain current as a function of drain - to - source voltage for steps in the gate 2 to source voltage. The vertical scale is .05 mA/ division, the horizontal scale is 2V/division, and the step increment is 1.0V with the last step at -6.2V.





(c)





(d)

Figure 10 (continued)

be improved via the existence of gate G3. However, if the control voltage on gate G3 is further increased to adjust the transconductance, as in the case of dual gate devices [21], the output resistance of the last two I-V curves shown in Fig. 10(c) corresponding to V_{G2} = -5.2 volts and -6.2 volts decreases due to channel length modulation under gate G3 where the current I_D is limited by this channel. This illustrates that it is difficult to adjust the transconductance of this device by simply varying the gate voltage V_{G3} while keeping high output resistance. Indeed the transconductance can be easily adjusted by varying the gate voltage V_{G1} without degrading the output resistance.

It can be seen that some I-V curves shown in Fig. 10(d) are equally spaced. This phenomenon implies that the transconductance can be adjusted to be a constant value, independent of input gate voltage V_{G2}, in a certain operational range. Since the active load is commonly used in a basic amplifier and the inherent square law of the driver of the single gate MOSFET introduces some nonlinearity, the three gate device with constant transconductance can eliminate the distortion due to the square law nonlinearity. Furthermore, the presence of the G1 control gates could allow adjustment of the offset voltage of an operational amplifier. The transconductance g_m versus input gate voltages V_{G2} with V_{g1} as a parameter is plotted in Fig. 11, where V_{g3} is biased at -10 volts to maximize the output resistance and V_D at -20 volts to ensure that the three gate device is operated in the saturation region. Unlike the single gate MOSFET whose transconductance is proportional to the gate voltage, the three gate device has a constant transconductance in a certain input operational range which

depends on the control gate voltage V_{G1}.

The equivalent circuit of the trigate device may be modeled as a common source - common gate cascode arrangement. Such a configuration reduces the voltage gain of the first stage, hence reducing the Miller capacitance and improving the frequency response. The transistor corresponding to gate 1 may be considered to be simply a resistor as long as it is operating in the triode region of operation. In such a case it serves the role of negative feedback, thereby reducing the effective transconductance of the amplifier. If this transistor has an effective resistance R, then the effective transconductance is given by:

$$g_m = g_m'/(1+g_m'R) \qquad (9)$$

where g_m' is the transconductance of the transistor corresponding to gate 2. Clearly Eqn. (1) approaches 1/R if $g_m' R >> 1$. In this case, the g_m would be independent of the input gate voltage. This was in fact observed as shown over a limited range in Fig. 11.

At higher values of V_{g2} the g_m falls off either due to the transistor corresponding to gate 1 entering the saturation region or the transistor corresponding to gate 2 entering the triode region or both. Our simulation using a three transistor model for the three-gate device showed excellent agreement when the transfer curves of drain current vs. V_{G2} were plotted. Future design improvement to extend the range where g_m is constant can be made using such a model.

The three-gate MOSFET may be practical for analog integrated circuit applications. Gate lengths used in analog circuits are often larger than the minimum linewidth associated with a given technology, so that incorporation of a three-gate device with smallger gates is possible and does not result in a sacrifice of area.

III. Research in Other Areas

In addition to the accomplishments discussed in the previous section, progress has been made on the investigations of graded-index SiO_2 waveguides and of laser recrystallized silicon photodetectors formed on $LiNbO_3$ substrates. The concepts involved in these two areas have been described in program proposals and the previous interim report [23], so only a brief summary of progress will be given here.

For the first case, planar graded index SiO_2 optical waveguides characterized by very low scattering have been fabricated on silicon substrates. The waveguides were thermally grown on silicon in two different ways. In one case, a SiO_2 thickness of 15 microns resulted in waveguiding with a total waveguide attenuation of 0.6 dB/cm. In another case, intentional doping of the SiO_2 layer allowed waveguiding to take place at a thickness of 6.6 microns with a total waveguide attenuation of 2.3 dB/cm. In each case, the relatively small magnitude of the refractive index change suggests that coupling to the silicon substrate is an important loss mechanism. Measurements imply that scattering loss from the waveguide itself is exceedingly low, and that continuing efforts to increase the field confinement may result in waveguides characterized by a substantially smaller value for the total waveguide attenuation.

Regarding laser recrystallized photodetectors, progress has occurred, but the final result has not yet been achieved. Extensive experiments on laser recrystallization of polysilicon have taken place. Relatively large area crystal grains have been achieved by using some novel beam scanning techniques. Both wafer translation and beam

on/off switching have been computerized. For the photodetectors a mask set has been designed and fabricated. The fabrication process to be utilized incorporates local oxidation for detector isolation. This should also alleviate the requirements on the area of the crystal grains needed for fabrication of high quality photodetectors.

IV. Outlook - Progress with Regard to Objectives

Significant progress towards several of the objectives of the portion of the AFOSR research program for which this interim report applies has been accomplished. Photodetection in which the electrical signal is proportional to the logarithm of the incident light intensity has been demonstrated over a dynamic range of almost 70 dB. The sensor element which performs this log conversion is suitable for incorporation into a linear CCD imaging array. As a part of this study a three gate MOSFET which provides independent control of transconductance and output resistance was demonstrated. Enhancement of quantum efficiency in edge-illuminated photodetectors at near IR wavelengths was also demonstrated. This method of illumination occurs naturally with photodetectors integrated with optical waveguide structures. Significant progress has been reported on graded-index SiO_2 waveguides exhibiting low scattering. Further work is needed, however, to simultaneously achieve strong field confinement, effective substrate isolation, and low scattering. In the area of photodetectors formed from laser recrystallized polysilicon, some progress has been reported, but further work is underway to actually demonstrate such devices having good performance. Once this capability is achieved, it will allow formation of silicon photodetector arrays on any optical waveguide substrate, thus achieving integration of photodetector arrays with general optical waveguide structures.

At the present time research in this program is continuing, as described in our most recent proposal.

V. List of Program Publications: AFOSR 81-0130

S.H. Chang and J.T. Boyd, "A Log-Converting Photosensor Element for Linear CCD Image Arrays," to be published.

H.E. Jackson, D.E. Zelmon, J.T. Boyd, and P.B. Kosel, "Fabrication of a Graded-Index SiO_2 Planar Optical Waveguide on Silicon Exhibiting Low Scattering," presented at and published in The Proceedings of the Society of Photoinstrumentation Engineers Meeting, Arlington, Virginia, April, 1983.

J.T. Boyd, "Microfabrication Techniques for Integrated Optics," presented at and published in the Proceedings of Electro/83, New York, April, 1983.

S.H. Chang, J.T. Boyd, and J.H. Nevin, "Three Gate MOSFET Providing Independent Control of Transconductance and Output Resistance," IEEE Electron Device Letters, to be published.

C.L. Fan and J.T. Boyd, "Improvement in the Quantum Efficiency of Silicon Photodetectors at Near IR Wavelengths by Edge Illumination," to be published.

D.E. Zelmon, H.E. Jackson, J.T. Boyd, A. Naumaan, and D.B. Anderson, "A Low-Scattering Graded-Index SiO_2 Planar Optical Waveguide Thermally Grown on Silicon," Applied Physics Letters, Vol. 42, pp. 565-566, April 1, 1983.

S. Dutta, H.E. Jackson, J.T. Boyd, and C.W. White, "Rutheford Back Scattering (RBS) Evidence for Solid Phase Laser Annealing of Corning 7059 Glass and ZnO Thin Films," Journal of Applied Physics, Vol. 54, pp. 2125-2126, April, 1983.

S. Dutta, H.E. Jackson, and J.T. Boyd, "Use of Laser Annealing to Achieve Low Loss in Corning 7059 Glass, ZnO, Si_3N_4, Nb_2O_5, and Ta_2O_5 Optical Thin-Film Waveguides," Optical Engineering, Vol. 22, pp. 117-120, January, 1983.

S. Dutta, H.E. Jackson, and J.T. Boyd, "Use of Laser Annealing to Achieve Low Loss in Corning 7059 Glass, ZnO, Si_3N_4, Nb_2O_5, and Ta_2O_5 Optical Thin-Film Waveguides," presented at and published in the Proceedings of the Society of Photoinstrumentation Engineers Meeting, Los Angeles, January, 1982.

C.L. Fan, "Improvement in the Performance of Silicon Photodetectors Used in Integrated Optics by Edge Illumination and Optical Waveguide Integration" Ph.D. Dissertation, University of Cincinnati, 1983.

S. Dutta, H.E. Jackson, J.T. Boyd, F.S. Hickernell and R.L. Davis, "Scattering Loss Reduction in ZnO Optical Waveguides by Laser Annealing," Applied Physics Letters, Vol. 39, pp. 206-208, Aug. 1, 1981.

A. Naumaan, D. Zelmon, and J.T. Boyd, "A thick SiO_2 Graded-Index Planar Waveguide," presented at and published in the Proceedings of the 31st Electronic Components Conference, Atlanta, May 11-13, 1981.

F.S. Hickernell, R.L. Davis, S. Dutta, J.T. Boyd and H.E. Jackson, "Optical Waveguide Loss Reduction in Zinc Oxide Films by Laser Annealing," presented at and published in the Proceedings of the AIME Electronic Materials Conference, Santa Barbara, June 24-26, 1981.

S.H. Chang, "A Logarithmic Photodetector Sensor Element for Charge-Coupled Device Imagers," Ph. D. Dissertation, University of Cincinnati, 1982.

H. Lu, "CO_2 Laser Recrystallization of Polysilicon and Annealing of MIS Devices," MS Thesis, University of Cincinnati, 1982.

S. Dutta, J.T. Boyd, and H.E. Jackson, "Laser Annealing of ZnO Optical Waveguides," presented at the Meeting of the American Physical Society, Dallas, March, 1982.

S. Dutta, H.E. Jackson, and J.T. Boyd, "Use of Laser Annealing to Achieve Low Loss in Corning 7059 Glass, ZnO, Si_3N_4, Nb_2O_5, and Ta_2O_5 Optical Thin-Film Waveguides," presented at and published in the Proceedings of the Society of Photoinstrumentation Engineers Meeting, Los Angeles, January, 1982.

S. Dutta, H.E. Jackson, J.T. Boyd, R.L. Davis, and F.S. Hickernell, "CO_2 Laser Annealing of Si_3N_4, Nb_2O_5, and Ta_2O_5 Thin Film Waveguides to Reduce Optical Scattering," IEEE Journal of Quantum Electronics, Vol. QE-18, pp 800-806, April, 1982, Joint Special Issue on Optical Guided Wave Technology, also published in IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-30, April, 1982.

J.T. Boyd, S. Dutta, H.E. Jackson, and A. Naumaan, "Reduction of the Effects of Scattering by Laser Annealing of Optical Waveguides and by Use of Integrated Waveguide Detection," Optical Engineering, Vol. 21, pp. 293-295, 1982.

F.K. Hopkins, H.E. Jackson, and J.T. Boyd, "In-Plane Scattering Measurements in a Planar Optical Waveguide by an Integrated Technique," Applied Optics, Vol. 20, pp. 2761-2763, Aug. 15, 1981.

S. Dutta, "Reduction of Scattering in Thin-Film Optical Waveguides by Carbon Dioxide Laser Annealing," Ph.D. Dissertation, University of Cincinnati, 1981.

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VII. References

1. J. T. Boyd, D. A. Ramey, C. L. Chen, A. Naumaan, S. Dutta, and S. H. Chang, "Integration of a Detector Array With An Optical Waveguide Structure and Applications to Signal Processing," Final Report, AFOSR-76-3032, Aug. 7, 1981.

2. S. H. Chang and J. T. Boyd, "A Log-Converting Photosensor Element For Linear CCD Image Arrays," to be published.

3. S. H. Chang, J. T. Boyd, and J. H. Nevin, "Three Gate MOSFET Providing Independent Control of Transconductance and Output Resistance," to be published.

4. C. L. Fan and J. T. Boyd, "Improvement in the Quantum Efficiency of Silicon Photodetectors at Near IR Wavelengths by Edge Illumination," to be published.

5. H. E. Jackson, D. E. Zelmon, J. T. Boyd, and P. B. Kosel, "Fabrication of a Graded-Index SiO_2 Planar Optical Waveguide on Silicon Exhibiting Low Scattering," to be presented at and published in The Proceedings of the Society of Photoinstrumentation Engineers Meeting, Arlington, Virginia, April, 1983.

6. D. E. Zelmon, H. E. Jackson, J. T. Boyd, A. Naumaan, and D. B. Anderson, "A Low-Scattering Graded-Index SiO_2 Planar Optical Waveguide Thermally Grown on Silicon," Applied Physics Letters 42, 565 (1983).

7. M. C. Hamilton, D. A. Wille, and W. J. Miceli, "An Integrated Optical RF Spectrum Analyzer," Optical Engineering 16, 475 (1977).

8. D. B. Anderson, J. T. Boyd, M. C. Hamilton, and R. R. August, "Integrated Optics Approach to the Fourier Transform," IEEE Journal of Quantum Electronics, Vol. QE-13, pp 268-275, April 1977, Special Issue on Integrated Optics.

9. M. K. Barnoski, B. V. Chen, T. R. Joseph, J. Y. M. Lee, and O. G. Ramer, "Integrated-Optic Spectrum Analyzer," IEEE Trans. on Circuits and Systems CAS-26, 1113 (1979).

10. D. Mergerian, E. C. Malarkey, R. P. Pautienus, J. C. Bradley, G. E. Marx, L. D. Hutcheson, and A. L. Kellner, "Operational Integrated Optical RF Spectrum Analyzer," Appl. Opt. 19, pp 3033-3034, 1980.

11. T. G. Giallorenzi, J. A. Bucaro, A. Dandridge, G. H. Sigel, Jr., J. H. Cole, S. C. Rashleigh, and R. G. Priest, "Optical Fiber Sensor Technology," IEEE Journal of Quantum Electronics, Vol. QE-18, p. 626, 1982.

12. M. F. Tompsett and C. H. Sequin, Charge Transfer Devices, Academic Press, 1975.

13. R. H. Dyck, "Design, Fabrication, and Performance of CCD Imagers," VLSI Electronics Microstructure Science, Edited by N. G. Einspruch, Vol. 3, pp. 65-107, 1982.

14. R. Rappaport, "The Photovoltaic Effect and Its Utilization," RCA Rev., Vol. 21, pp. 373-397, 1959.

15. C. H. Sequin and A. M. Mohsen, "Linearity of Electrical Charge Injection into Charge-Coupled Devices," IEEE Journal of Solid-State Circuits, Vol. SC-10, pp. 81-92, 1975.

16. G. M. Borsuk, "Photodetectors for acousto-optic signal processors," Proc. IEEE, Vol. 69, pp. 100-118, 1981.

17. W. C. Dash and R. Newman, "Intrinsic optical absorption in single crystal germanium and silicon at 77°K and 300°K," Phys. Rev., Vol. 99, pp. 1151-1155, 1955.

18. J. K. Rodman and J. T. Boyd, "Examination of CCDs using voltage constrast with a scanning electron microscope," Solid-State Electron. Vol. 23, pp. 1029-1033, 1980.

19. S. M. Sze, Physics of Semiconductor Devices, New York: Wiley, 1981, p. 749.

20. EG&G Data Sheet, EG&G, Inc.

21. R. M. Barsan, "Analysis and Modeling of Dual-Gate MOSFET's," IEEE Trans. Electr. Dev., Vol. ED-28, pp. 523-533, 1981.

22. R. R. Troutman and H. S. Lee, "Inversion Charge Transistor (ICT) for Better Threshold Control in Small Dimensions," IEEE J. Sol. St. Circ., Vol. SC-13, pp. 490-491, 1978.

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